

REMARKS

Claims 1 to 5, 7 to 15, 17 to 25 and 27 to 30 are pending in the application, of which claims 1, 11 and 21 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

In the Office Action, claims 4, 14 and 24 were objected to for the reason noted on page 2, and the abstract was objected to for including legal phraseology. As shown above, Applicants have amended the abstract and claims 4, 14 and 24 to attend to the objections. Withdrawal of the objections is therefore respectfully requested.

Claims 1 to 10 were rejected under 35 U.S.C. §101 for allegedly being directed to nonstatutory subject matter. As shown above, Applicants have amended claim 1 to specify that its method is performed by a processing device. This amendment clearly puts claim 1, and dependent claims 2 to 10, within the technological arts. Accordingly, withdrawal of the §101 rejection is respectfully requested.

Claims 1 to 3, 7, 9, 10, 11 to 13, 17, 19, 20, 21 to 23, 27, 29 and 30 were rejected under §102(b) over U.S. Patent No. 5,220,512 (Watkins); claims 4 to 6, 14 to 16, and 24 to 26 were rejected under §103 over Watkins in view of U.S. Patent No. 6,480,985 (Reynolds); and claims 8, 18 and 28 were rejected under §103 over Watkins in view of U.S. Patent No. 5,544,067 (Rostoker). As shown above, Applicants have amended the claims to define the invention with greater clarity. In view of these clarifications, withdrawal of the art rejections is respectfully requested.

Amended independent claim 1 defines a method, performed by a processing device, for simulating a logic design having combinatorial logic and state logic, which includes

representing the combinatorial logic and the state logic using separate graphic elements, identifying clock domains for the combinatorial logic and the state logic using the separate graphic elements, generating computer code that simulates operation of portions of the logic design, the computer code being generated based on the clock domains, and associating the computer code with graphic elements that correspond to the portions of the logic design

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, the applied art is not understood to disclose or to suggest at least identifying clock domains for combinatorial logic and state logic using separate graphic elements, generating computer code based on the clock domains that simulates operation of portions of a logic design, and associating the computer code with graphic elements

In this regard, Watkins describes a system for simulating logic designs that utilizes graphic elements to represent elements of the logic design, and that provides a table of values indicating the output of each graphic element. It was said on page 5 of the Office Action that Watkins Fig. 3 and column 9, lines 55 to 59 describe generating computer code based on clock domains. Applicants respectfully disagree with this characterization of Watkins. Rather, as understood by Applicants, the cited portion of Watkins merely describes producing a macro that simulates a clock to apply to the simulation. Watkins, however, does not disclose generating computer code based on clock domains. That is, in Watkins, the computer code generates the clock, whereas in the invention, the computer code is generated based on an existing clock domain – quite the opposite of Watkins.

Reynolds and Rostoker likewise are not understood to disclose or to suggest the foregoing features of claim 1, nor were they cited for their disclosure of clock domains.

For at least the foregoing reasons, claim 1 is believed to be patentable over the art. Amended independent claim 11 is an article of manufacture claim that roughly corresponds to claim 1; and amended independent claim 21 is an apparatus claim that roughly corresponds to claim 1. Claims 11 and 21 are also believed to be patentable over the art for at least the same reasons noted above with respect to claim 1.

Regarding, Reynolds, it was said on pages 6 and 7 of the Office Action that Reynolds describes using C++ to graphically represent an IC design and, therefore, claims reciting the use of C++ code were obvious variants of Watkins and Reynolds. Applicants respectfully disagree. In this regard, Reynolds does not disclose or suggest use of C++ code to simulate operation of portions of a logic design. Instead, as noted in column 8, lines 41 et seq. of Reynolds, C++ code is used to generate a graphical representation of an IC design, not its operation (see also Fig. 6 of Reynolds). For at least this reason, Applicants submit that all claims reciting use of C++ distinguish even further over the art.

In this regard, each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, all dependent claims have not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments

made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

Please apply any fees or credits due in this case to Deposit Account 06-1050, referencing Attorney Docket No. 10559-597001.

Respectfully submitted,

Date: May 19, 2005



Paul A. Pysher
Reg. No. 40,780

Attorneys for Intel Corporation
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906
21028884.doc